

## BACKGROUND OF THE INVENTION

The present invention relates in general to a television (referred to hereinafter as TV)-integrated video cassette recorder (referred to hereinafter as VCR) apparatus, and more particularly to a TV-integrated digital VCR apparatus in which a digital VCR is interfaced with a high definition television (referred to hereinafter as HDTV) or a standard TV to record and play back data of a HDTV format or of a standard TV format.

A standard TV system such as, for example, an NTSC system has generally been used till now, while a HDTV system has recently been developed and will be commercially available in the near future. Although the HDTV system will be commercially available, it is anticipated that the standard TV system will coexist with the HDTV system for a long time.

On the other hand, compatibility is required between the standard TV system and the HDTV system in the case where a digital VCR intends to record an NTSC broadcasting signal as well as a HDTV broadcasting signal, to convert the HDTV broadcasting signal into the NTSC broadcasting signal for playback or to convert the NTSC broadcasting signal into the HDTV broadcasting signal for the playback.

For example, trick playback modes of the NTSC system such as edit & dubbing, a high-speed playback and etc. are difficult to perform with a HDTV broadcasting signal format. For this reason, there is a necessity for efficiently applying the trick playback modes of the NTSC system to the HDTV system. Also, recording modes of the NTSC system such as a standard play (SP), a long play (LP) and etc. must readily be applied to the HDTV system.

Therefore, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a TV-integrated VCR apparatus which is capable of recording and playing back both a HDTV broadcasting signal and a standard TV broadcasting signal to provide compatibility between a standard TV system and a HDTV system.

In accordance with the present invention, the above and other objects can be accomplished by a provision of a television-integrated video cassette recorder apparatus comprising a high definition television for receiving a high definition television signal from a broadcasting station; a digital video cassette recorder for recording and playing back the high definition television signal or a standard television signal on/from a magnetic tape; and interface means for converting a format of the high definition television signal into a recording format of said digital video cassette recorder in a recording mode, converting a format of a playback signal from said digital video cassette recorder into a high definition television format or a standard television format in a playback mode and performing a plurality of screen processing functions in a standard television manner. Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating

preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a TV-integrated VCR apparatus in accordance with the embodiments of the present invention;

FIG. 2 is a detailed block diagram of a format converter in an interface circuit in FIG. 1;

FIGS. 3A and 3B are views illustrating data scanning conversion manners in accordance with the present invention;

FIG. 4 is a view illustrating a data region size conversion manner in accordance with the present invention;

FIG. 5 is a signal waveform diagram obtained by the data region size conversion manner in FIG. 4;

FIG. 6 is a view illustrating an example of a data region division manner in accordance with the present invention;

FIG. 7 is a detailed block diagram of a sub-sampler of a sampling circuit in the interface circuit in FIG. 1;

FIG. 8 is a detailed block diagram of an up-sampler of the sampling circuit in the interface circuit in FIG. 1;

FIG. 9 is a detailed block diagram of a post-processor in the interface circuit in FIG. 1;

FIG. 10 is a detailed block diagram of an encoder in a digital VCR in FIG. 1;

FIGS. 11A to 11C are views illustrating data scanning format conversion manners in accordance with the present invention;

FIG. 12 is a detailed block diagram of a formatter in the digital VCR in FIG. 1; and

FIGS. 13A to 13C are views illustrating sequentially a data recording format conversion manner in accordance with the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, there is shown a block diagram of a TV-integrated VCR apparatus in accordance with the embodiments of the present invention. As shown in this drawing, the TV-integrated VCR apparatus comprises a HDTV 100 for receiving a HDTV signal HDi from a broadcasting station, a digital VCR 200 for recording and playing back the HDTV signal or a standard TV signal on/from a magnetic tape, and an interface circuit 300 for converting a format of the HDTV signal into a recording format of the digital VCR 200 in a recording mode, converting a format of a playback signal from the digital VCR 200 into a HDTV format or a standard TV format in a playback mode and performing various screen processing functions in a standard TV manner.

The HDTV 100 includes a tuner 1 for tuning the HDTV signal HDi from the broadcasting station, a demodulator 2 for demodulating an output V1 from the tuner 1, correcting a mixed error component of the demodulated signal and separating a video signal V2 and an audio signal A2 from the

The interface circuit 300 includes a format conversion circuit 9 for converting a format of video data from the HDTV 100 or the digital VCR 200 into a desired format, a sampling circuit 10 for sub-sampling video outputs Y1', U1' and V1', Y2', U2' and V2' and Y3', U3' and V3' from the format conversion circuit 9 to reduce a data amount thereof, outputting the sampled signals to the digital VCR 200, up-sampling video outputs Y", U" and V" from the digital VCR 200 to increase a data amount thereof and outputting the sampled signals to the format conversion circuit 9, a post-processor 11 for processing video outputs Yo, Uo and Vo from the format conversion circuit 9 to perform the various screen processing functions such as a picture-in-picture (PIP) function, a zooming function, an edit function and etc., a D/A converter 12 for converting video outputs YP, UP and VP from the post-processor 11 into an analog video signal and outputting the analog video signal to a standard TV monitor Monitor 2, an analog audio output unit 8 for inputting an analog audio signal from the digital VCR 200 through a switch SW5 and outputting the inputted analog audio signal to a speaker SP2, and a digital audio input/output unit 7 for inputting and outputting digital audio signals from/to the HDTV 100 and the digital VCR 200 through switches SW1 and SW4.

The playback part of the digital VCR 200 includes a playback amplifier/equalizer circuit 20 for amplifying a signal detected by heads HD3 and HD4 by a predetermined level and compensating for a distortion of the amplified signal, a channel demodulator 21 for demodulating an output V20 from the amplifier/equalizer circuit 20, a defor-

matter/error correction decoder (ECD) circuit 22 for converting a format of an output V21 from the channel demodulator 21 into an original format and correcting an error component of the converted signal, and a decoder 23 for decoding video and audio outputs V22 and A22 from the deformatter/error correction decoder circuit 22 into original signals Yd, Ud, Vd and A23 and outputting the video signals through the switch SW3 to a D/A converter 24 for the playback in the standard TV manner or to the sampling circuit 10 in the interface circuit 300 for the playback in the HDTV manner. The D/A converter 24 is adapted to convert the video and audio outputs Yd, Ud and Vd and A23 from the decoder 23 into analog video and audio signals and output the analog video and audio signals to a standard TV display unit.

Referring to FIG. 2, there is shown a detailed block diagram of the format conversion circuit 9 in the interface circuit 300. As shown in this drawing, the format conversion circuit 9 includes a synchronous frequency-divider 31 for frequency-dividing a synchronous signal Sync, a clock frequency-divider 32 for frequency-dividing a clock CLK, a clock detector 33 for discriminating a format of input video data Y, U and V in response to an output from an OR gate OR1 which inputs the clock CLK and a format select mode signal MSM, a format identifier (ID) read only memory (ROM) 36 for storing identifier data regarding digital data formats, a phase locked loop (PLL) 35 for adjusting a phase of an oscillating frequency in response to an output V36 from the format identifier ROM 36, a buffer 37 for buffering the motion vector M.V and the displaced frame or field difference signal DFD from the decoder 3 in the HDTV 100, and a scanning format determinator 38 for outputting scanning conversion control data IPDD in accordance with levels of the motion vector M.V and displaced frame or field difference signal DFD buffered by the buffer 37.

Also, the format conversion circuit 9 includes a format controller 34 for outputting a format control signal V34 in response to the scanning conversion control data IPDD from the scanning format determinator 38 and an output from the clock detector 33, a scanning format converter 25 for performing progressive/interlaced scanning conversion or interlaced/progressive scanning conversion with respect to the input video data Y, U and V in response to the format control signal V34 from the format controller 34, an output Vsync from the synchronous frequency-divider 31 and an output VCLK from the clock frequency-divider 32, a format region converter 26 for converting a size of video output data Yi, Ui and Vi from the scanning format converter 25 or video output data Yc, Uc and Vc from a digital camera into a desired size, a video divider 27 for dividing video output data Yo, Uo and Vo from the format region converter 26 by regions, and buffers 28-30 for buffering video outputs Y1, U1 and V1, Y2, U2 and V2 and Y3, U3 and V3 from the video divider 27, respectively.

Referring to FIG. 7, there is shown a detailed block diagram of a sub-sampler 101 of the sampling circuit 10 in the interface circuit 300. As shown in this drawing, the sub-sampler 101 includes low pass filters (LPFs) 391-399 for removing high frequency components from the video outputs Y1', U1' and V1', Y2', U2' and V2' and Y3', U3' and V3' from the format conversion circuit 9, respectively, sub-sampler elements 401-409 for sub-sampling outputs V391-V399 from the low pass filters 391-399, respectively, and video synthesizers 411-413 for synthesizing Y components, U components and V components of outputs V401-V409 from the sub-sampler elements 401-409 to reform them into the video signals Y'', U'' and V'' and

outputting the reformed video signals Y", U" and V" to the encoder 15 in the digital VCR 200 through the switch SW3, respectively.

Referring to FIG. 8, there is shown a detailed block diagram of an up-sampler 102 of the sampling circuit 10 in the interface circuit 300. As shown in this drawing, the up-sampler 102 includes video dividers 421-423 for receiving the video signals Y", U" and V" from the digital VCR 200 through the switch SW3 in the playback mode and dividing the received video signals by regions, respectively, up-sampler elements 431-439 for up-sampling outputs from the video dividers 421-423, respectively, and low pass filters (LPFs) 441-449 for removing high frequency components from outputs V431-V439 from the up-sampler elements 431-439 and outputting the resultant video signals to the buffers 28-30 in the format conversion circuit 9, respectively.

Referring to FIG. 9, there is shown a detailed block diagram of the post-processor 11 in the interface circuit 300. As shown in this drawing, the post-processor 11 includes a format converter 46 for converting a HDTV format of the video outputs Yo, Uo and Vo from the format conversion circuit 9 into an NTSC format, a picture zoomer 47 for adjusting a size of a video to be displayed, an art processor 48 for performing an art process such as the video edit function, a color inverter 49 for performing a color inverting function, and a synthesizer 50 for synthesizing Y components, U components and V components of outputs Y46, U46 and V46 from the format converter 46, outputs Y47, U47 and V47 from the picture zoomer 47, outputs Y48, U48 and V48 from the art processor 48 and outputs Y49, U49 and V49 from the color inverter 49 to reform them into the video signals YP, UP and VP and outputting the reformed video signals YP, UP and VP to the D/A converter 12. Here, the format converter 46, the picture zoomer 47, the art processor 48 and the color inverter 49 are controlled in response to an output V45 from a mode selector 45, the synchronous signal Sync and the clock signal CLK.

Referring to FIG. 10, there is shown a detailed block diagram of the encoder 15 in the digital VCR 200. As shown in this drawing, the encoder 15 includes a formatting circuit 500 for formatting data inputted therein and a coding circuit 600 for scrambling output data from the formatting circuit 500 and coding the scrambled data.

The formatting circuit 500 includes a formatter 51 for receiving the video outputs YN, UN and VN from the A/D converter 14 or the video outputs Y", U" and V" from the sub-sampler 101 in the interface circuit 300 through the switch SW3 and dividing the received signals into odd and even field data Vodd and Veven, field memories 52 and 53 for storing the odd and even field data Vodd and Veven from the formatter 51, respectively, an adder 54 for adding outputs V52 and V53 from the field memories 52 and 53, and an interlaced/progressive (I/P) formatter 55 for formatting an output V54 from the adder 54 and the outputs V52 and V53 from the field memories 52 and 53 according to scanning conversion information IPDI.

The coding circuit 600 includes a scramble controller 59 for generating a scramble control signal V59 in response to a scramble protection key signal and an output from a scramble map table 58 and outputting the generated scramble control signal V59 to a frame buffer 56 and a scrambler 57.

The frame buffer 56 is adapted to temporarily store an output V55 from the I/P formatter 55 in the formatting circuit 500 in response to the scramble control signal V59 from the scramble controller 59.

The scrambler 57 is adapted to scramble an output V56 from the frame buffer 56 in response to the scramble control signal V59 from the scramble controller 59.

Also, the coding circuit includes a discrete cosine transform (DCT) unit 61 for performing a DCT operation with respect to an output V57 from the scrambler 57, an activity calculator 62 for calculating an activity of an output V61 from the DCT unit 61, a control parameter calculator 63 for calculating a control parameter V63 in response to an output V62 from the activity calculator 62, a control parameter initializer 64 being initialized in response to the calculated control parameter V63 from the control parameter calculator 63, a delay element 65 for delaying the output V61 from the DCT unit 61 for a predetermined time period, and a data selector 66 for selecting an output V65 from the delay element 65 in response to an output Vth from the control parameter initializer 64 if it is greater than a threshold level and outputting the selected data to a human visual system (HVS) unit 67.

The human visual system unit 67 is adapted to select a human visual system matched with a video characteristic of an output V66 from the data selector 66 in response to an output Vpi from the control parameter initializer 64 and multiply DCT coefficients of the output V66 from the data selector 66 by a weight function corresponding to the selected human visual system.

A quantizer 69 is adapted to quantize an output V67 from the human visual system unit 67 in response to an output Vsf from the control parameter initializer 64.

A variable length coder (VLC) 70 is adapted to perform variable length coding with respect to an output V69 from the quantizer 69 in response to information from a field based VLC table 71, information from a frame based VLC table 72 and scanning conversion information IPDI' from a buffer 60 which buffers the scanning conversion information IPDI.

The coding circuit 600 also includes a buffer 73 for buffering a coded bit stream V70 from the variable length coder 70 and applying its output Vc to the error correction coder 16, and a coding controller 68 for checking an output rate of the buffer 73 and controlling the data selector 66 and the quantizer 69 in accordance with the checked result to prevent generation of an overflow or an underflow in the coded bit stream or the output Vc from the buffer 73, thereby to make the coding stable.

Referring to FIG. 12, there is shown a detailed block diagram of the formatter 17 in the digital VCR 200. As shown in this drawing, the formatter 17 includes a segment separator 74 for separating the synchronous signal Sync and data information from each segment of a data bit stream or the output V16 from the error correction coder 16. The segment is a minimum unit of data to be read in a multispeed playback.

Also, the formatter 17 includes a data memory 75 for storing the data information from the segment separator 74, a header appender 76 for appending an identifier and status information to the synchronous signal Sync from the segment separator 74 in the unit of segment in response to an interleaving control signal ICS, and a demultiplexer 78 for demultiplexing an output V75 from the data memory 75 in the unit of segment in response to the interleaving control signal ICS and outputting the demultiplexed signals to buffers 791-79n, respectively.

The formatter 17 also includes delay elements 801-80n for delaying outputs B1-Bn from the buffers 791-79n for different predetermined time periods, respectively, a multi-

On the other hand, in the case where the standard TV broadcasting signal NTSC from the broadcasting station is received by the digital VCR 200, it is tuned to a desired channel and then demodulated by the tuner/demodulator circuit 13. Also, the tune/demodulator circuit 13 corrects the error component mixed into the broadcasting signal during the transmission and separates the video signal NVi and the audio signal NAI from the error-corrected signal. The A/D converter 14 converts the video and audio signals NVi and NAI from the tuner/demodulator circuit 13 into the digital signals. The resultant audio signal A14 from the A/D converter 14 is applied directly to the encoder 15 and the

resultant video signals YN, UN and VN therefrom are applied through the switch SW3 to the encoder 15.

In the encoder 15, as shown in FIG. 10, the formatter 51 receives the video signals YN, UN and VN from the A/D converter 14 through the switch SW3 and divides the received signals into the odd and even field data V<sub>odd</sub> and V<sub>even</sub>, which are then stored into the field memories 52 and 53, respectively. The adder 54 adds the output data V<sub>52</sub> and V<sub>53</sub> from the field memories 52 and 53 and outputs the added data V<sub>54</sub> to the I/P formatter 55, which also receives the output data V<sub>52</sub> and V<sub>53</sub> from the field memories 52 and 53.

The I/P formatter 55 formats the output data V<sub>54</sub> from the adder 54 and the output data V<sub>52</sub> and V<sub>53</sub> from the field memories 52 and 53 into frame, even field and odd field blocks according to the scanning conversion information IPDI, respectively, as shown in FIG. 11A.

On the other hand, the scramble controller 59 reads scramble information from the scramble map table 58 in response to the scramble protection key signal set by the user and generates the scramble control signal V<sub>59</sub> in accordance with the read scramble information. The scramble control signal V<sub>59</sub> from the scramble controller 59 is applied to the frame buffer 56 and the scrambler 57.

The frame buffer 56 stores temporarily the output V<sub>55</sub> from the I/P formatter 55 in response to the scramble control signal V<sub>59</sub> from the scramble controller 59 and outputs the stored signal to the scrambler 57. Then, under the control of the scramble controller 59, the scrambler 57 scrambles the output data V<sub>56</sub> from the frame buffer 56 according to a desired rule. With this scrambling process, the output data V<sub>56</sub> from the frame buffer 56 becomes uniform in length, resulting in a reduction of a burst error component. This uniformity also makes the control of the buffer 73 easy. On the other hand, provided that a key input signal is different from the scramble protection key signal previously set by the user, the scrambling of the scrambler 57 is not performed normally, resulting in formation of an undesirable video.

Then, the DCT coefficients of the output V<sub>57</sub> from the scrambler 57 are obtained by the DCT operation of the DCT unit 61 and applied to the activity calculator 62. The activity calculator 62 obtains the activity of the DCT coefficients from the DCT unit 61 by summing absolute values thereof. On the basis of the obtained activity V<sub>62</sub> from the activity calculator 62, the control parameter calculator 63 calculates the control parameter V<sub>63</sub> and outputs the calculated control parameter V<sub>63</sub> to the control parameter initializer 64, thereby causing the control parameter initializer 64 to be initialized. As a result of the initialization, the control parameter initializer 64 outputs the control signals V<sub>th</sub>, V<sub>pi</sub> and V<sub>sf</sub> to the data selector 66, the human visual system unit 67 and the quantizer 69, respectively.

The output V<sub>61</sub> from the DCT unit 61 is also delayed by the delay element 65 for the predetermined time period and then applied to the data selector 66. The data selector 62 functions to select the output data V<sub>65</sub> from the delay element 65 in response to the control output V<sub>th</sub> from the control parameter initializer 64 if it is greater than the threshold level and output the selected data V<sub>66</sub> to the human visual system unit 67. The human visual system unit 67 selects the human visual system matched with the video characteristic of the output V<sub>66</sub> from the data selector 66 in response to the control output V<sub>pi</sub> from the control parameter initializer 64. Then, the human visual system unit 67 multiplies the DCT coefficients of the output V<sub>66</sub> from the data selector 66 by the weight function corresponding to the



The output **V75** from the data memory **75** is demultiplexed into signals **DM1-DMn** in the unit of segment by the demultiplexer **78** according to the interleaving control signal **ICS**. The demultiplexed outputs **DM1-DMn** from the demultiplexer **78** are buffered by the buffers **791-79n** and then delayed for the different predetermined time period by the delay elements **801-80n**, respectively. Noticeably, the

difference in the delay time periods of the segments results in 90°-rotation of each segment as shown in FIG. 13B. Namely, the difference in the delay time periods of the segments results in no discontinuity of the segments. As a result, a track deviation of the heads has no effect on detection of an information amount by the heads although it is produced in a multispeed playback mode. Therefore, a good picture quality can be obtained in the multispeed playback mode.

Subsequently, the multiplexer 81 multiplexes the outputs D11-D1n from the delay elements 801-80n in response to the interleaving control signal ICS. The output V81 from the multiplexer 81 is interleaved into the new format through an inter-symbol interleaving process by the interleaver 82 depending on the interleaving control signal ICS. As a result, the interleaver 82 outputs the signal V82 tough against the burst error component as shown in FIG. 13C. Then, the segment reformatter 77 formats the output V76 from the header appender 76 and the output V82 from the interleaver 82 into the recording format of the digital VCR 200 and outputs the resultant data stream to the channel modulator 18 in FIG. 1.

The channel modulator 18 modulates the output V17 from the formatter 17 suitably to the characteristic of the magnetic tape and the channel characteristic. Then, the output V18 from the channel modulator 18 is amplified by the predetermined level by the recording amplifier 19 and recorded on the magnetic tape through the heads HD1 and HD2 being switched by a switch SW7.

On the other hand, in the case where the HDTV signal HDi received by the HDTV 100 is to be recorded in the digital VCR 200, the audio signal A2 from the demodulator 2 in the HDTV 100 of FIG. 1 is applied to the digital audio input/output unit 7 in the interface circuit 300 through the switch SW1, and the video signal V2 therefrom is decoded by the decoder 3 and then applied to the format conversion circuit 9 in the interface circuit 300 through the switches SW2 and SW6.

In the format conversion circuit 9, as shown in FIG. 2, the clock detector 33 discriminates the format of the input video data Y, U and V or Yc, Uc and Vc in response to the output from the OR gate OR1 which inputs the clock CLK and the format select mode signal MSM. Then, the PLL 35 adjusts the phase of the oscillating frequency in response to the output V36 from the format identifier ROM 36 corresponding to the format discriminated by the clock detector 33, and outputs the phase-adjusted oscillating frequency V35 to the clock detector 33. As a result, the format controller 34 outputs the format control signal V34 in response to the output V33 from the clock detector 33, thereby allowing the scanning format converter 25 to perform the progressive/interlaced scanning conversion with respect to the input video data Y, U and V or Yc, Uc and Vc to reduce band widths thereof if the format is the progressive scanning type, while to pass them through a switch SW9 if the format is the interlaced scanning type. On the other hand, the synchronous signal Sync and the clock CLK are frequency-divided by the synchronous frequency-divider 31 and the clock frequency-divider 32, respectively, suitably to the recording format of the digital VCR 200.

In other words, if the format of the input video data Y, U and V or Yc, Uc and Vc is the progressive scanning type, the scanning format converter 25 converts the input video data Y, U and V or Yc, Uc and Vc of the progressive scanning type into the video data Yi, Ui and Vi of the interlaced scanning type as shown in FIG. 3A, and outputs the con-

verted video data  $Y_i$ ,  $U_i$  and  $V_i$  to the format region converter 26. On the contrary, if the format of the input video data  $Y$ ,  $U$  and  $V$  or  $Y_c$ ,  $U_c$  and  $V_c$  is the interlaced scanning type, the scanning format converter 25 passes the video data  $Y$ ,  $U$  and  $V$  or  $Y_c$ ,  $U_c$  and  $V_c$  of the interlaced scanning type to the format region converter 26 through the switch SW9.

As shown in FIG. 4, the format region converter 26 converts a size  $(X, Y)$  of the input video data into a desired size  $(X', Y')$  by performing a down-sampling operation. Namely, as shown in FIGS. 4 and 5, if  $X/X' > 1$ ,  $Y/Y' > 1$  and  $\text{Int}(n \cdot X/X') < n \cdot X/X' < \text{Int}(n \cdot X/X' + 1)$ , the  $Z'n$  can be obtained as follows:

$$Z'N = [n \cdot X/X' - \text{Int}(n \cdot X/X')] \cdot Z_{\text{Int}(n \cdot X/X' + 1)} + [\text{Int}(n \cdot X/X' + 1) - n \cdot X/X'] \cdot Z_{\text{Int}(n \cdot X/X')} \quad (1)$$

With the above equation (1), the size  $(X, Y)$  of the input video data can readily be converted into the desired size  $(X', Y')$ .

The video output data  $Y_o$ ,  $U_o$  and  $V_o$  from the format region converter 26 are applied to the video divider 27 through a switch SW 10. The video divider 27 divides the received video data into a plurality of parts  $Y_1$ ,  $U_1$  and  $V_1$ ,  $Y_2$ ,  $U_2$  and  $V_2$  and  $Y_3$ ,  $U_3$  and  $V_3$  according to a video importance as shown in FIG. 6. Then, the buffers 28-30 buffer the video outputs  $Y_1$ ,  $U_1$  and  $V_1$ ,  $Y_2$ ,  $U_2$  and  $V_2$  and  $Y_3$ ,  $U_3$  and  $V_3$  from the video divider 27, respectively, and output the buffered video data  $Y_1'$ ,  $U_1'$  and  $V_1'$ ,  $Y_2'$ ,  $U_2'$  and  $V_2'$  and  $Y_3'$ ,  $U_3'$  and  $V_3'$  to the sub-sampler 101 of the sampling circuit 10 in FIGS. 1 and 7, respectively. Also, the video output data  $Y_o$ ,  $U_o$  and  $V_o$  from the format region converter 26 are applied through the switch SW10 to the post-processor 11 in FIGS. 1 and 9.

In the post-processor 11, as shown in FIG. 9, the video output data  $Y_o$ ,  $U_o$  and  $V_o$  from the format region converter 26 in the format conversion circuit 9 are processed by the format converter 46, the picture zoomer 47, the art processor 48 and the color inverter 49 under the control of the mode selector 45. As a result, the PIP function, the zooming function, the art processing function and the color inverting function can be performed by the format converter 46, the picture zoomer 47, the art processor 48 and the color inverter 49, respectively. Then, the synthesizer 50 synthesizes the  $Y$  components,  $U$  components and  $V$  components of the outputs  $Y_{46}$ ,  $U_{46}$  and  $V_{46}$  from the format converter 46, the outputs  $Y_{47}$ ,  $U_{47}$  and  $V_{47}$  from the picture zoomer 47, the outputs  $Y_{48}$ ,  $U_{48}$  and  $V_{48}$  from the art processor 48 and the outputs  $Y_{49}$ ,  $U_{49}$  and  $V_{49}$  from the color inverter 49 in response to the synchronous signal Sync, respectively. In result, the synthesized video outputs  $Y_P$ ,  $U_P$  and  $V_P$  from the synthesizer 50 are converted into the analog video signal by the D/A converter 12 in FIG. 1 and then outputted to the standard TV monitor Monitor2.

Namely, the post-processor 11 acts to display the HDTV broadcasting signal in the NTSC manner or perform the PIP function, the zooming function, the art processing function and etc. of the NTSC broadcasting signal. Therefore, the post-processor 11 provides the compatibility between the HDTV system and the NTSC TV system.

On the other hand, in the sub-sampler 101, as shown in FIG. 7, the low pass filters 391-399 remove the high frequency components from the video outputs  $Y_1'$ ,  $U_1'$  and  $V_1'$ ,  $Y_2'$ ,  $U_2'$  and  $V_2'$  and  $Y_3'$ ,  $U_3'$  and  $V_3'$  from the format conversion circuit 9, respectively, to limit frequency bands thereof for prevention of a video overlapped phenomenon. Then, the sub-sampler elements 401-409 sub-sample the outputs  $V_{391}$ - $V_{399}$  from the low pass filters 391-399,

respectively, to reduce the data amount thereof. Noticeably, the filtering and sub-sampling are performed to allocate more information to important video portions, while less information to unimportant video portions. Therefore, the data can efficiently be compressed.

Then, the outputs V401, V404 and V407 from the sub-sampler elements 401, 404 and 407 are applied to the video synthesizer 411 through output terminals P1, P4 and P7 thereof and input terminals P1', P4' and P7' of the video synthesizer 411. Also, the outputs V402, V405 and V408 from the sub-sampler elements 402, 405 and 408 are applied to the video synthesizer 412 through output terminals P2, P5 and P8 thereof and input terminals P2', P5' and P8' of the video synthesizer 412. Further, the outputs V403, V406 and V409 from the sub-sampler elements 403, 406 and 409 are applied to the video synthesizer 413 through output terminals P3, P6 and P9 thereof and input terminals P3', P6' and P9' of the video synthesizer 413. In response to the synchronous signal Sync, the clock CLK and a control signal CTL, the video synthesizers 411-413 synthesize the Y components, U components and V components of the outputs V401-V409 from the sub-sampler elements 401-409 to reform them into the original video signals Y", U" and V", respectively.

In other words, the video data Y, U and V from the HDTV 100 or the video data Yc, Uc and Vc from the digital camera are converted into the video data Y", U" and V" of the interlaced scanning type as shown in FIG. 11B by the interface circuit 300. Then, the video data Y", U" and V" of the interlaced scanning type from the interface circuit 300 are applied to the encoder 15 through the switch SW3.

In the encoder 15, the formatter 51 divides the received video data Y", U" and V" of the interlaced scanning type into the odd and even field data Vodd and Veven, which are then stored into the field memories 52 and 53, respectively. The adder 54 adds the output data V52 and V53 from the field memories 52 and 53 and outputs the added data V54 to the I/P formatter 55, which also receives the output data V52 and V53 from the field memories 52 and 53.

The I/P formatter 55 formats the output data V54 from the adder 54 and the output data V52 and V53 from the field memories 52 and 53 into interlaced macro blocks or progressive macro blocks according to the scanning conversion information IPDI, and outputs the formatted blocks to the frame buffer 56. FIG. 11C shows examples of the interlaced macro blocks and the progressive macro blocks. The output data from the frame buffer 56 is coded in the compression manner suitable to the digital VCR 200 through the subsequent procedure of the encoder 15, which is similar to that in the case where the NTSC signal is received by the digital VCR 200 as mentioned previously and details thereof will thus be omitted.

Then, the error correction coder 16 receives the video output V15 from the encoder 15 directly and the audio signal A7 from the digital audio input/output unit 7 through the switch SW4 and corrects the error components of the received video and audio signals. The formatter 17 formats the output V 16 from the error correction coder 16 into the recording format of the digital VCR 200 and the channel modulator 18 modulates the output V17 from the formatter 17 suitably to the characteristic of the magnetic tape and the channel characteristic. Then, the output V18 from the channel modulator 18 is amplified by the predetermined level by the recording amplifier 19 and recorded on the magnetic tape through the heads HD1 and HD2 being switched by the switch SW7.

On the other hand, in the case where the recorded HDTV or standard TV signal is to be played back in the standard TV

In the format conversion circuit **9**, as shown in FIG. 2, the clock detector **33** discriminates the format of the input video data in response to the output from the OR gate **OR1** which inputs the clock **CLK** and the format select mode signal **MSM**. Then, the PLL **35** adjusts the phase of the oscillating frequency in response to the output **V36** from the format

identifier ROM 36 corresponding to the format discriminated by the clock detector 33, and outputs the phase-adjusted oscillating frequency V35 to the clock detector 33.

The synchronous signal Sync is frequency-divided by the synchronous frequency-divider 31 suitably to the HDTV format. The format controller 34 controls the scanning format converter 25, the format region converter 26 and the video divider 27 in response to the output V33 from the clock detector 33.

Upon receiving the outputs Y1', U1' and V1', Y2', U2' and V2' and Y3', U3' and V3' from the up-sampler 102, the buffers 28-30 buffer the received signals, respectively, and output the buffered signals to the video divider 27. In this case, the video divider 27 acts to synthesize the video portions divided for the recording according to the video importance. Namely, the video divider 27 converts the received video signals into the video signals Yo, Uo and Vo of the desired size (X', Y'). Then, the outputs Yo, Uo and Vo from the video divider 27 are applied to the format region converter 26 or the post-processor 11 through the switch SW10.

In the case where the outputs Yo, Uo and Vo from the video divider 27 are applied to the post-processor 11 of FIG. 9 through the switch SW10, they are processed by the format converter 46, the picture zoomer 47, the art processor 48 and the color inverter 49 under the control of the mode selector 45. Then, the synthesizer 50 synthesizes the Y components, U components and V components of the outputs Y46, U46 and V46 from the format converter 46, the outputs Y47, U47 and V47 from the picture zoomer 47, the outputs Y48, U48 and V48 from the art processor 48 and the outputs Y49, U49 and V49 from the color inverter 49 in response to the synchronous signal Sync, respectively. In result, the synthesized video outputs YP, UP and VP from the synthesizer 50 are converted into the analog video signal by the D/A converter 12 in FIG. 1 and then outputted to the standard TV monitor Monitor2.

In the case where the outputs Yo, Uo and Vo from the video divider 27 are applied to the format region converter 26 through the switch SW10, they are up-sampled by the format region converter 26 for conversion into the size (X, Y). Then, the scanning format converter 25 receives the video signals Yi, Ui and Vi of the interlaced scanning type from the format region converter 26 through the switch SW9 and converts the received video signals into the video signals Y, U and V of the progressive scanning type as shown in FIG. 3B. At this time, the format controller 34 controls the scanning format converter 25 to perform inter-field interpolation or intra-field interpolation using the scanning conversion information based on the motion vector and the displaced frame or field difference signal used in the previous encoding. Namely, the scanning format converter 25 converts the video signals Yi, Ui and Vi of the interlaced scanning type into the video signals Y, U and V of the progressive scanning type by performing the inter-field interpolation or the intra-field interpolation under the control of the format controller 34.

Subsequently, the video processor 4 receives the expanded video signals Y, U and V from the format conversion circuit 9 and restores the received video signals into the original color signals R, G and B. Then, the D/A converter 5 converts the color signals R, G and B from the video processor 4 into the analog video signal and outputs the converted analog video signal to the high definition monitor Monitor1. On the other hand, the audio signal A7 is applied to the decoder 3 through the digital audio input/output unit 7 and then to the D/A converter 6. Then, the D/A